FM1033

3P3T Switch with MIPI for 0.4 to 5.0G

Features

- Multi-Band operation 0.4 to 5.0GHz
- Excellent insertion loss
- 0.55dB Insertion Loss at 1.0GHz
- 0.75dB Insertion Loss at 2.7GHz
- 0.90dB Insertion Loss at 3.8GHz
- Input 0.1dB compression point: 36dBm
- MIPI RFFE V2.1 interface compatible
- Compact 2.0mm x 2.0mm x 0.55 mm QFN-16 package, MSL

Applications

- Simultaneous voice and LTE systems
- Antenna switching

Description

The FM1033 is a CMOS, high isolation, Silicon-On-Insulator (SOI) three-pole, three -throw (3P3T) switch. The switch provides high linearity performance, low insertion loss and high isolation.

The FM1033 is compatible with MIPI control, which is a key requirement for many cellular transceivers. RF1, RF3, RF5 pins connect to one of the three other RF port pins (RF2 or RF4 or RF6) through a low insertion loss path, while maintaining a very high isolation path to the other ports. No external DC blocking capacitors are required on the RF path as long as no DC voltage is applied externally.

The FM1033 high isolation 3P3T switch is provided in a QFN (16-pin, 2.0 x 2.0 x 0.55 mm) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 1, too. Signal pin assignments and functional pin descriptions are provided in Table 1.

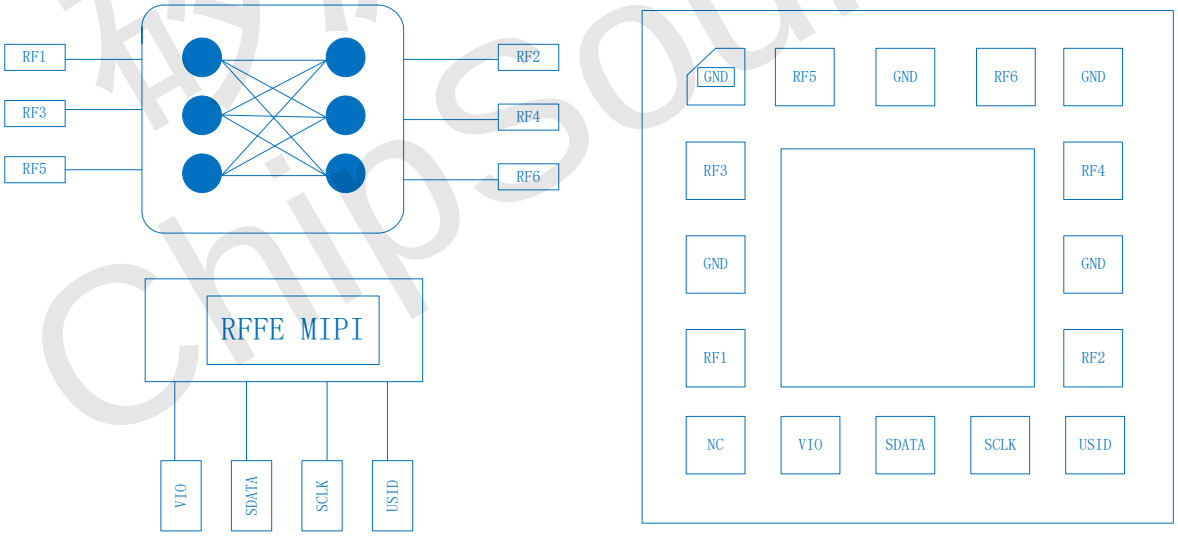


Figure 1 Functional Block Diagram and Pin Configuration

Function Characteristic

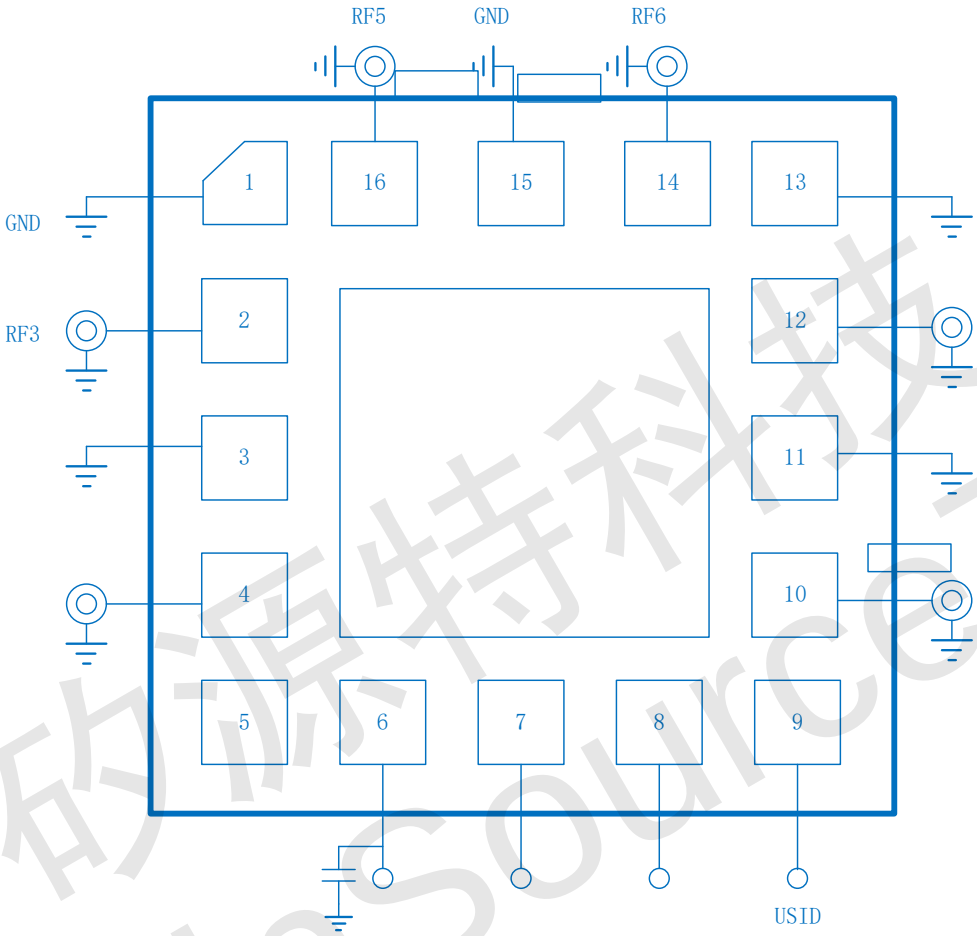


Figure 2 FM1033 Application Circuit

Table 1 Pin Descriptions

NO.	Name	Description	NO.	Name	Description
1	GND	Ground	9	USID	RFFE Slave ID Select Pin
2	RF3	RF Port 3	10	RF2	RF Port 2
3	GND	Ground	11	GND	Ground
4	RF1	RF Port 1	12	RF4	RF Port 4
5	NC	Not Connected	13	GND	Ground
6	VIO	Supply Voltage	14	RF6	RF Port 6
7	SDATA	RFFE Data Bus	15	GND	Ground
8	SCLK	RFFE Clock Bus	16	RF5	RF Port 5

Table 2 Register_0 & Register_1 for RF Operating Modes

State	Mode	Register_0							
		D7	D6	D5	D4	D3	D2	D1	D0
1	RF5 ISO	x	x	x	x	x	0	0	0
2	RF5 – RF6	x	x	x	x	x	0	0	1
3	RF5 – RF4	x	x	x	x	x	0	1	0
4	RF5 – RF2	x	x	x	x	x	1	0	0
5	RF3 ISO	x	x	0	0	0	x	x	x
6	RF3 – RF6	x	x	0	0	1	x	x	x
7	RF3 – RF4	x	x	0	1	0	x	x	x
8	RF3 – RF2	x	x	1	0	0	x	x	x

State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
1	RF1 ISO	x	x	x	x	x	0	0	0
2	RF1 – RF6	x	x	x	x	x	0	0	1
3	RF1 – RF4	x	x	x	x	x	0	1	0
4	RF1 – RF2	x	x	x	x	x	1	0	0

Notice

x—Either 0 or 1 which means the device supports multi-channel-on operational modes

Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{IO}	-0.3	2.5	V	T_A=25℃
RFFE Bus Voltage (SDATA, SCLK)	V_I	-0.3	2.5		T_A=25℃
USID Control Voltage	V_{USID}	-0.3	2.5		T_A=25℃
Max RF Input Power (RF1/3/5 to TRX2/4/6)	P_{INMAX}		36	dBm	F_0=0.6 to 5.0GHz, CW, V_{IO}=1.8V, VSWR=1:1, TA=25℃
Device Operating Temperature	T_{OP}	-40	90	℃	
Device Storage Temperature	T_{STG}	-55	150		
Electrostatic Discharge (All Pins)	$V_{ESD(HBM)}$	1000		V	Human Body Model
	$V_{ESD(CDM)}$	1000			Charged Device Model

Notice

Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Table 4 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Frequency	F_0	0.4		5.0	GHz
Power Supply for MIPI	V_{IO}	1.65	1.8	1.95	V
RFFE Bus Voltage (SDATA, SCLK) High	V_{IH}	0.8*VIO	VIO	VIO	
RFFE Bus Voltage (SDATA, SCLK) Low	V_{IL}	0	0	0.2*VIO	
USID Control Voltage	V_{USID}	0		VIO	

Table 5 Nominal Operating Parameters

Parameter	Symbol	Specification			Unit	Condition
		MIN	TYP	MAX		
Normal Conditions	V_{IO}=1.8V, V_{IH}=1.8, V_{IL}=0V, P_{IN}=0dBm, VSWR=1:1, T_A=25℃, Unless Otherwise Stated					
DC Performances						
Current on VIO	I_{IO}		260	360	μA	
Timing Performances						
RF Path Switching Time (One On Path to Another)	T_{SW}		2	3	μs	RF Switching CMD Implemented (50% SCLK) to 90%/10% RF Applied
Wake Up Time	T_{WP}			20		Exiting Lower Power State CMD Implemented(50%SCLK) to 90% RF
Turn On Time	T_{ON}			10		Cold Start, 50% VDD or VIO (the latter one to power up) to 90% RF
VIO Reset Time	T_{VIO_RST}	10				VIO Off to it starts to re-power up to trigger POR
RF Performances						
Insertion Loss (RF1/3/5 to RF2/4/6)	IL		0.55 0.65 0.75 0.90 1.40	0.65 0.75 0.90 1.40 1.80	dB	F_0=699 to 960MHz F_0=1.4 to 2.2GHz F_0=2.3 to 2.7GHz F_0=3.3 to 4.2GHz F_0=4.2 to 5.0GHz
Isolation (RF1/3/5 to RF2/4/6)	ISO	30 25 22 18 17	35 30 25 20 20			F_0=699 to 960MHz F_0=1.4 to 2.2GHz F_0=2.3 to 2.7GHz F_0=3.3 to 4.2GHz F_0=4.2 to 5.0GHz
Input Return Loss (RF1/3/5 to RF2/4/6)	RL	20 16 14 8 8	22 21 20 13 12			F_0=699 to 960MHz F_0=1.4 to 2.2GHz F_0=2.3 to 2.7GHz F_0=3.3 to 4.2GHz F_0=4.2 to 5.0GHz
Input 0.1 dB Compression Point (RF1/3/5 to RF2/4/6)	$P_{0.1dB}$		36		dBm	F_0=0.6 to 5.0GHz, CW
2nd Order Harmonic	$2F_0$		-60	-55		F_0=900MHz@35dBm
3rd Order Harmonic	$3F_0$		-51	-45		
2nd Order Harmonic	$2F_0$		-51	-48		F_0=1900MHz@33dBm

3rd Order Harmonic	$3F_0$		-50	-45		
2nd Order Harmonic	$2F_0$		-72	-65		F_0=950MHz@25dBm
3rd Order Harmonic	$3F_0$		-83	-75		

MIPI RFFE Read and Write Timing

MIPI RFFE V2.1 interface supports the following Command Sequences:

- Register Write
- Register Read
- Register_0 Write

Figure 3 and Figure 4 illustrate the timing diagrams for register write command sequence and read command sequence, respectively. Figure 5 describes the Register_0 write command sequence. In the below timing figures, SA[3:0] is the slave address. A[4:0] is the register address. D[7:0] is the data. “P” is a parity bit.

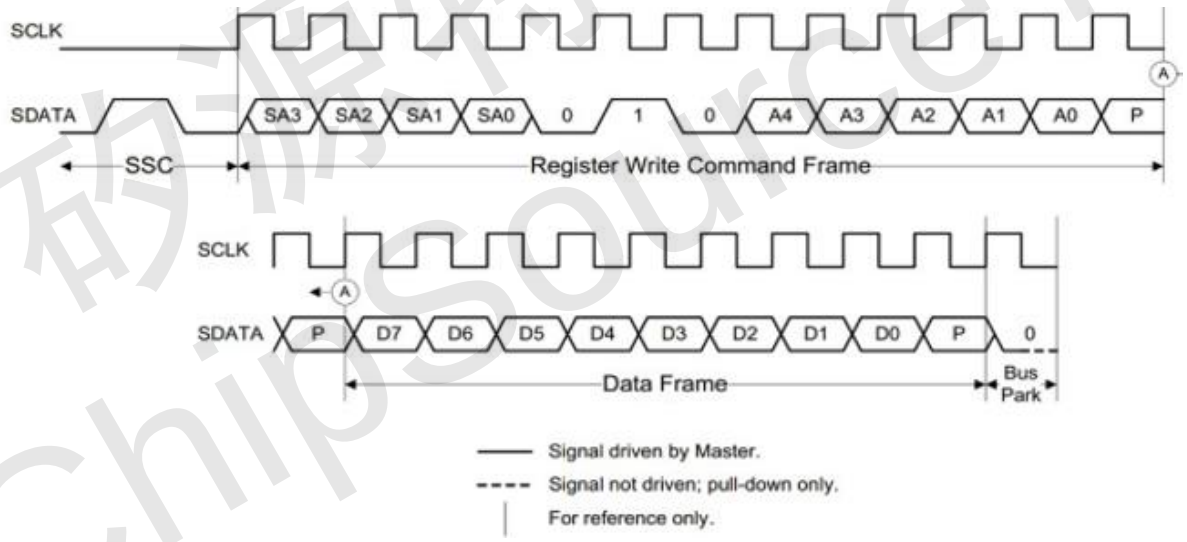


Figure 3 Register Write Command Sequence

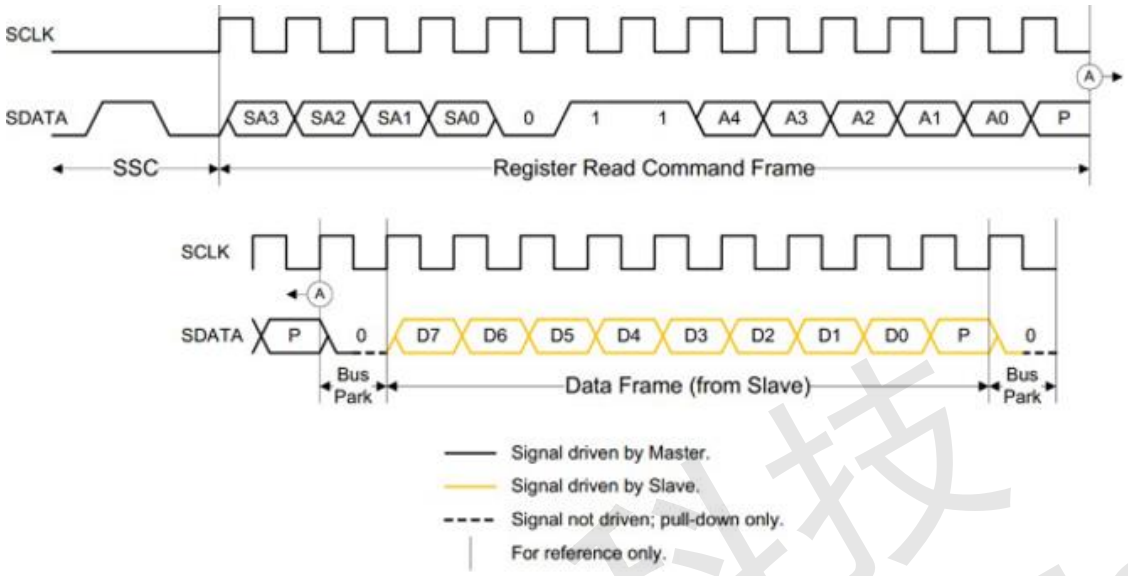


Figure 4 Register Read Command Sequence

Figure 5 shows the Register_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic '1' (to denote the command type and address), and an only seven- bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle.

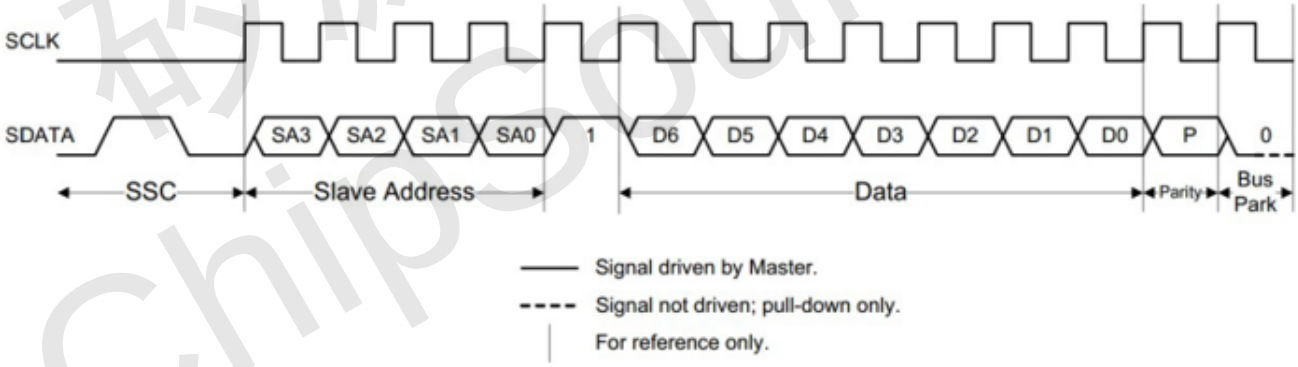


Figure 5 Register_0 Write Command Sequence

Other information such as MIPI USID programming sequence, MIPI bus specifications, etc. are started in the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V2.1(18-DEC-2017).

Register Definition

Table 6 Register Definition Table

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x00	REGISTER_0	7:0	R/W	RF Control 0	Register_0 Truth Table: Table 2	0x00	No	Yes
0x01	REGISTER_1	7:0	R/W	RF Control 1	Register_1 Truth Table: Table 2	0x00	No	Yes
0x1C	PM_TRIG	7	R/W	PWR_MODE_1	0b0: Normal Operation State Write Value:0b0, Read Value:0b0 0b1: Low Power State Write Value:0b1, Read Value:0b1	0b0	Yes	No
		6	R/W	PWR_MODE_0	0b0: Normal Operation (Active) 0b1: Reset all registers to default settings (Startup) Write value: 0b1, Read Value: 0b0	0b0	Yes	No
					Note: Writing PWR_MODE_0 with a logic '1' will reset all register, and then automatically reenter the ACTIVE Mode.			
		5	R/W	Trigger_Mask_2	0b0: Trigger_2 enabled 0b1: Trigger_2 disabled	0b0	No	No
		4	R/W	Trigger_Mask_1	0b0: Trigger_1 enabled 0b1: Trigger_1 disabled	0b0	No	No
		3	R/W	Trigger_Mask_0	0b0: Trigger_1 enabled 0b1: Trigger_1 disabled	0b0	No	No
		2	W	Trigger_2	0b0: Keep its associated destination registers unchanged 0b1: Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_2 is disabled(Logic '0')	0b0	Yes	No
		1	W	Trigger_1	0b0: Keep its associated destination registers unchanged 0b1: Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_1 is disabled(Logic '0')	0b0	Yes	No
		0	W	Trigger_0	0b0: Keep its associated destination registers unchanged 0b1: Load its associated destination registers with the data in the parallel shadow register, provided Trigger_Mask_0 is disabled(Logic '0')	0b0	Yes	No
0x1D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x0E	No	No

0x1E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x78	No	No
0x1F	MAN_USID	7:4	R	MANUFACTURER_ID[11:8]	Upper four bits of MIPI registered Manufacturer ID	0x2	No	No
		3:0	R/W	USID	Unique Slave ID		No	No
					USID pin connected to GND	0x8		
					USID pin connected to VIO	0x9		

MIPI RFFE Operating Sequences

Here are some recommendations for MIPI RFFE operating sequences to prevent the device from damage.

1) Basic Operational Sequences

- Power On -- Apply Supply (VIO)-> Apply MIPI RFFE Bus (SCLK & SDATA) -> Apply RF Signal
- Power Off -- Remove RF Signal-> Remove MIPI RFFE Bus (SCLK & SDATA)->Remove Supply (VIO)

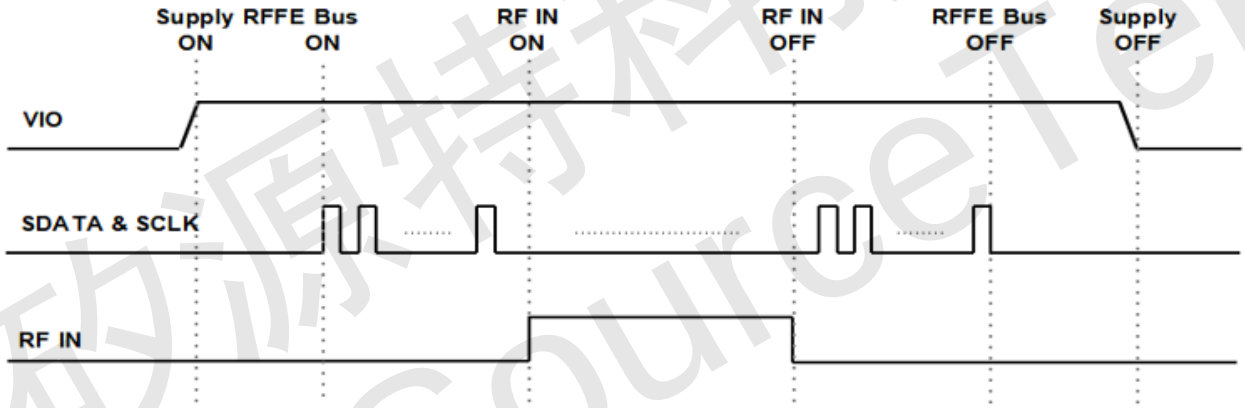


Figure 6 Basic Power On and Power Off Sequence

2) There shall be TON, after VIO powered on, before RF power is allowed to apply to any RF path.

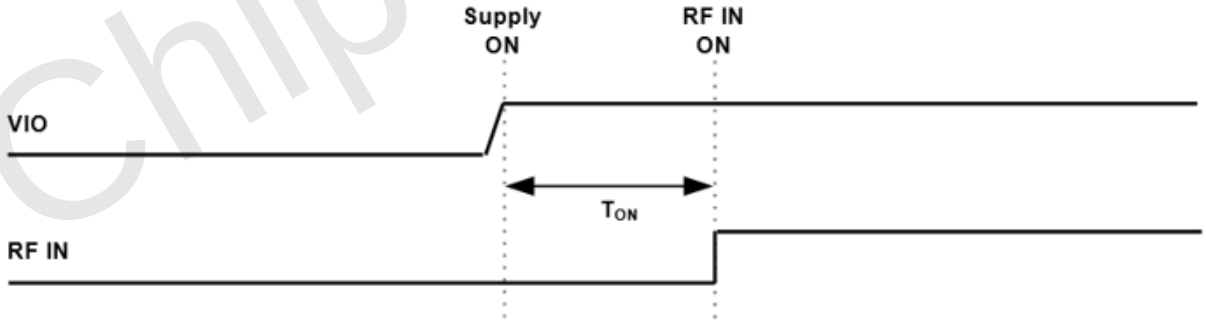


Figure 7 Supply and RF Signal On Sequence

3) To realize powered reset, after VIO enters the off state(VIO≤VVIO_RST=200mV), it shall take VIO TVIO_RST(≥ 10μs)to maintain the state before it is allowed to power up again. After then, VIO shall power up within TVIO_R(≤400μs) to trigger POR.

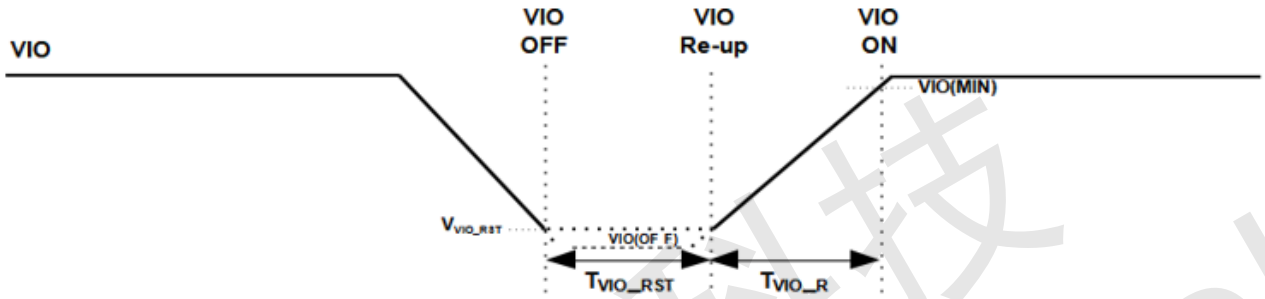


Figure 8 Powered Reset Sequence

4)To prevent the device from damage during switching events, RF signal shall be applied TSW after the switching command is implemented and removed TSW before any consequent switching command starts.

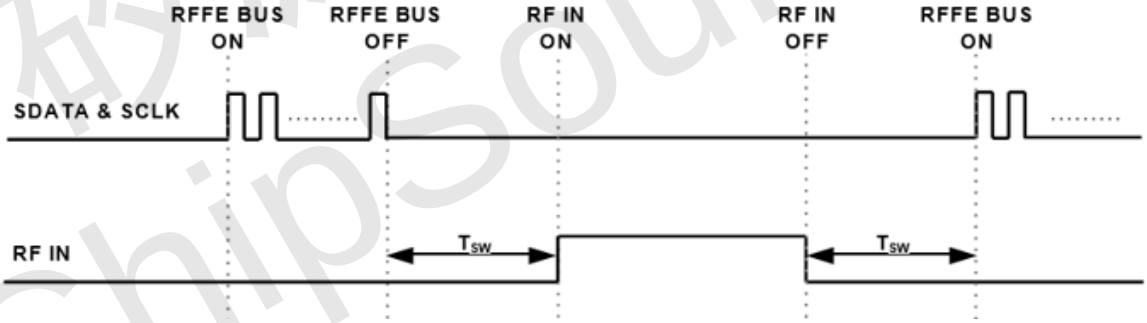


Figure 9 RF Path Switching Sequence

5) Large RF signal shall not be applied during low power state. Hence, it shall be removed before the device enters low power state. After the device is switched from low power state to active state, there shall be at least TWK(≥10μs) before RF signal can be applied again.

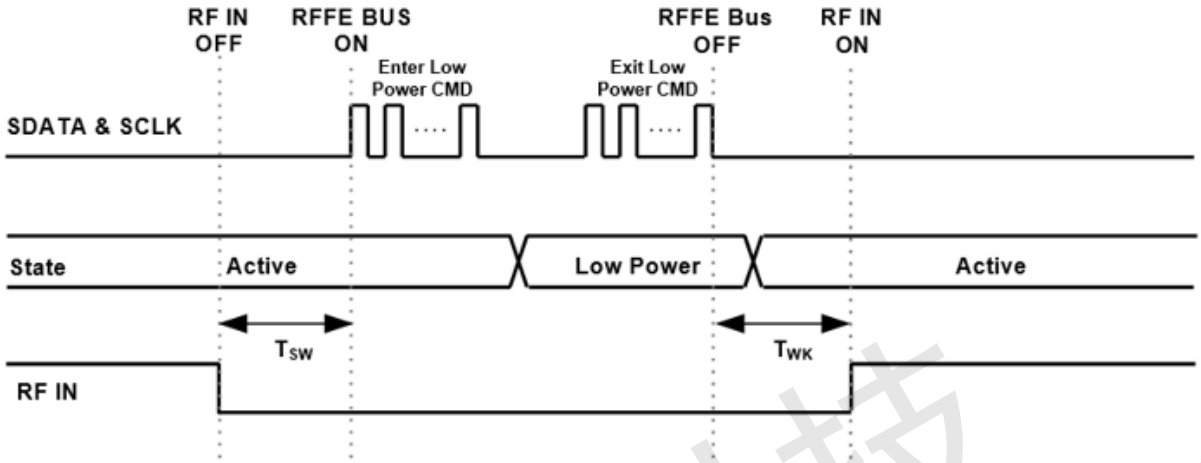
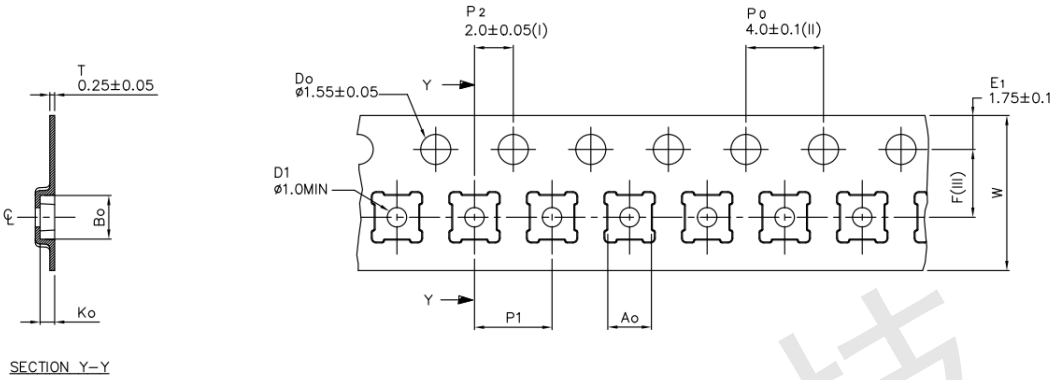


Figure 10 Enter and Exit Low Power State Sequence

Tape and Reel Dimensions



Ao	2.25 +/−0.1
Bo	2.25 +/−0.1
Ko	0.75 +/−0.1
F	3.50 +/−0.1
P1	4.00 +/−0.1
W	8.00 +/−0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 11 Tape and Reel Dimensions

Reflow Chart

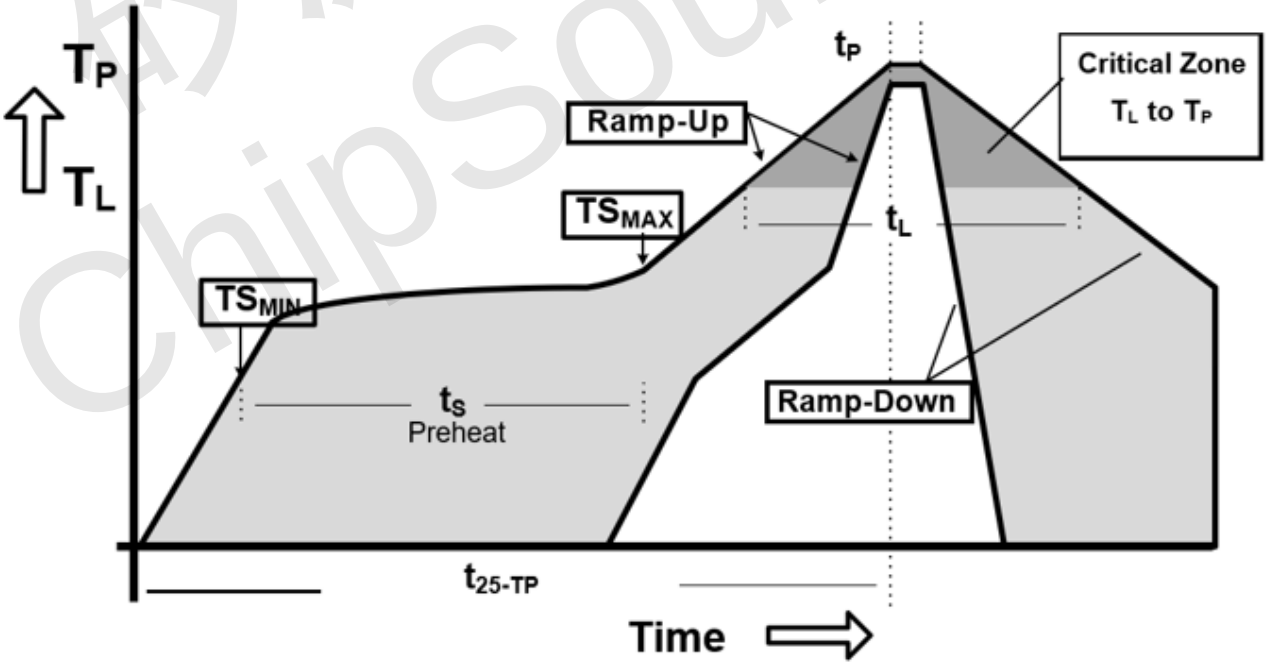


Figure 12 Recommended Lead-Free Reflow Profile

Table7 Reflow Chart Parameters

Reflow Profile	Parameter
Preheat Temperature(TS_{MIN} to TS_{MAX})	150℃ to 200℃
Preheat Time(ts)	60 to 180 Seconds
Ramp-Up Rate(TS_{MAX} to T_P)	3℃/s MAX
Time Above T_L 217℃(t_L)	60 to 150 Seconds
Peak Temperature (T_P)	260℃
Time within 5℃ of Peak Temperature(t_P)	20 to 40 Seconds
Ramp-Down Rate(TS_{MAX} to T_P)	6℃/s MAX
Time for 25℃ to Peak Temperature($t_{25\text{-}TP}$)	8 Minutes MAX

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operated.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.